APPLICATION NOTE

TDA8787A
INTERFACE FRONT END BOARD CAMERA
CAMDEMO 87A

AN 00012

Philips
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Summary

This application note describes on the one hand how to use the TDA8787A.

On the other hand, an example of application is given using an Interface Front End (IFE) board performed with a TDA8787A , a ¼ " medium resolution Sharp CCD sensor and its companion circuits.

The front-end board has been developed in such a way that it can be easily connected to an evaluation board of the Philips DSP family.
Associated with its sister DSP board built around the SAA8112, this IFE board gives an example of basic video camera application.

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1 IC FRONT END TDA8787A DESCRIPTION

1.1 General Description

The TDA8787A is a 3.3V, 10 bit analog-to-digital interface for CCD cameras.

TDA8787A is a low power, low supply voltage circuit which is able to operate from 2.7 volts to 3.6 volts.
Analog and digital supplies have several separated pins VCCA, VCCD and VCCO. Therefore special care must be taken when an application board is designed in order to avoid any external disturbing effect when using a non correct filtering circuit around these VCC's lines. See Chapter 3.

All digital inputs, as Standby inputs (STBY) and Output Enable Not (OE(N)) are TTL logic level compatible.
In addition, the outputs are CMOS level compatible. No adaptation circuits has been required to interface output data with CMOS family circuit working under the same value voltage of power battery.

Here is the list of the main functions implemented:

. Correlated Double Sampling circuit (CDS)
. Programmable Gain Amplifier(PGA)
. low power 10 bit Analog-to-Digital Converter
. integrated reference voltage regulator
. Serial Interface function for programming internal registers (SRI)
. 8 bit Digital-to-Analog Converter for extra external control function (OFD)
. Blanking interface
. Standby mode facilities

The TDA8787A has a 18 MHz maximum clock frequency.

Here is the CCD signal path:

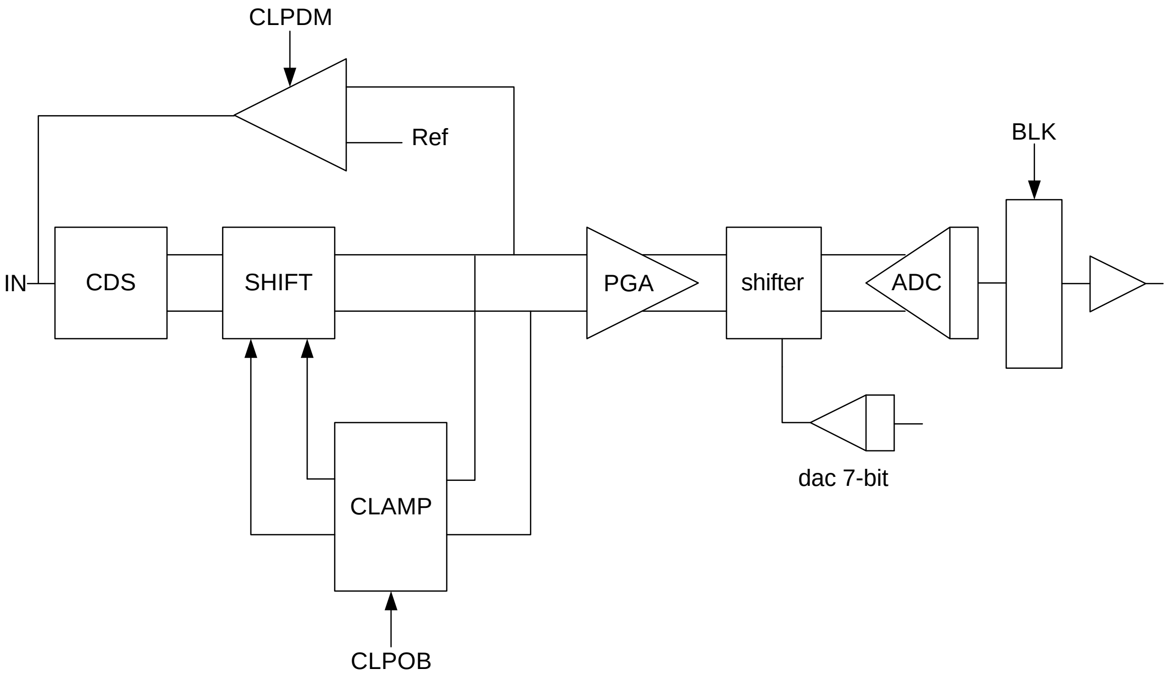
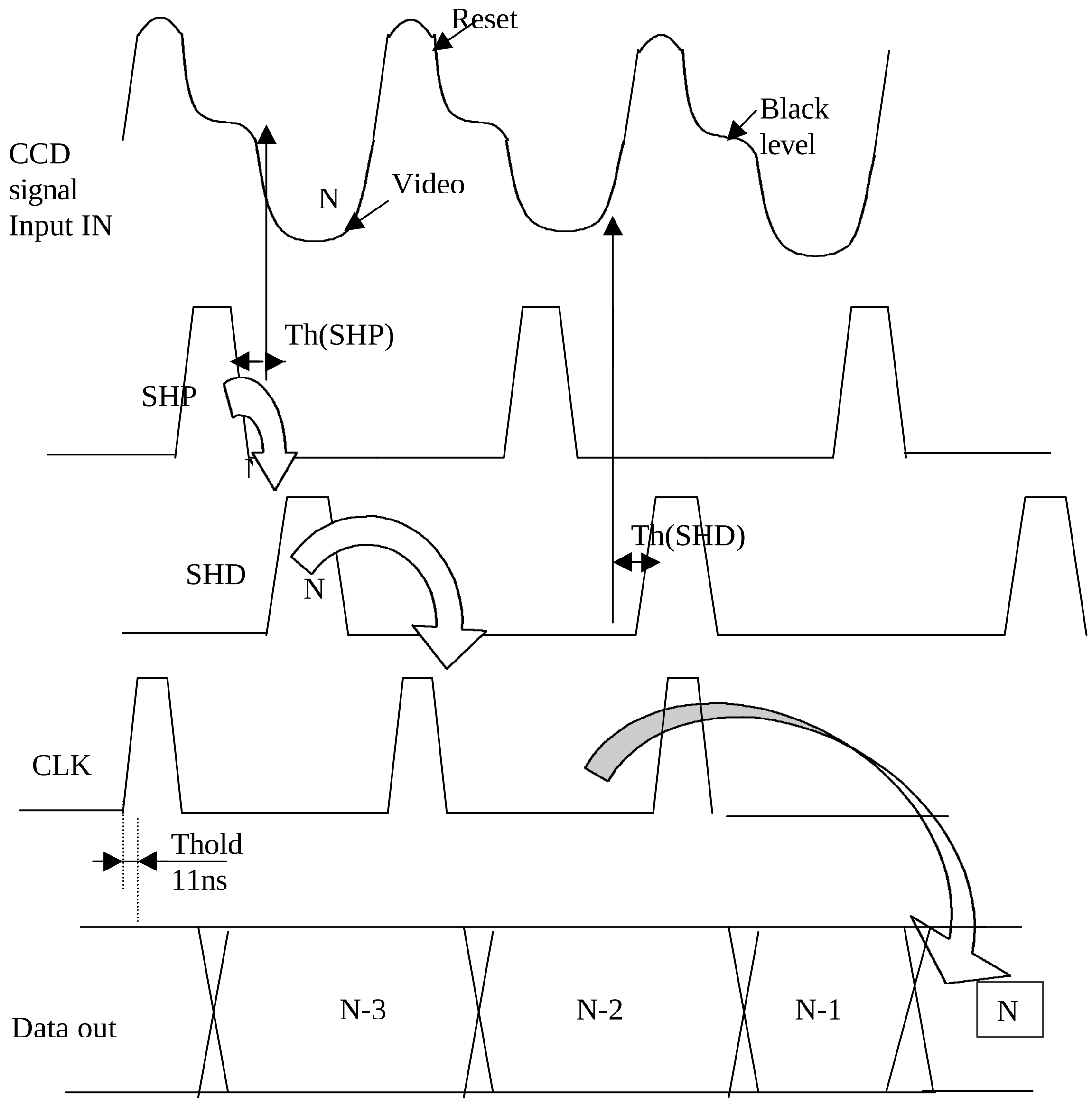


Figure 1. CCD signal path

1.2 Timing diagram

A typical input signal of CCD is depicted in Figure. 2, in comparison with SHP, SHD pulses, the Sample & Hold control pulses.
The CCD signal can be divided into three main parts, the reset gate pulse, the reset hold level (floating gate or black level) and the actual video level.

Figure 2. Typical CCD signal



Inside the TDA8787A, there is a pipeline delay between the external SHP and SHD signals present at the inputs and the actual internal switch action which samples the CCD signal. This delay is lower than 2 ns.
This delay has to be taken into account during the definition of an application diagram to make sure the video signal is correctly processed and no overlap exists between the different sampled periods (black and active video) and SHP, SHD control pulses.

1.3 Theory of operation

1.3.1 Correlated Double Sampling (CDS)

Figure 3. shows the simplify block diagram of the TDA8787A's CDS.
The CDS is required in CCD systems as a mean for removing several types of noises. With video information, reset noise, thermal noise, 1/f noise generated are present at the CCD output signal.
Since part of low frequencies noises are assumed to be correlated both during the active part of the video and during the feed through, major part of this noise can be cancelled by subtracting the feed through level from the video.

This classical technique known as Doubled Correlated Sampling uses SHP and SHD pulses to control the internal process of CDS. The timings of the operation is describe in the Fig 3&4 in the TDA8787A's Data Sheet.
During SHP period, the sample & hold goes into the hold mode, taking a sample of the reset level (floating gate level) including the noise. At time SHD, the second sample & hold takes a sample of the video level.
At the end, the result of this operation in the CDS is the generation of new signal which is now the true useful video level: Vreset – Vvideo. Then, this video level will be presented at the input of the digitally programmable gain amplifier tied down by DSP.
The TDA8787A actually uses two CDS circuits in a "ping pong" way. This method reduces the bandwidth per stage as compared to a single channel CDS. Thus, the output from one of the two CDS is valid for an entire clock cycle.

A and B are often named odd and even pixels.

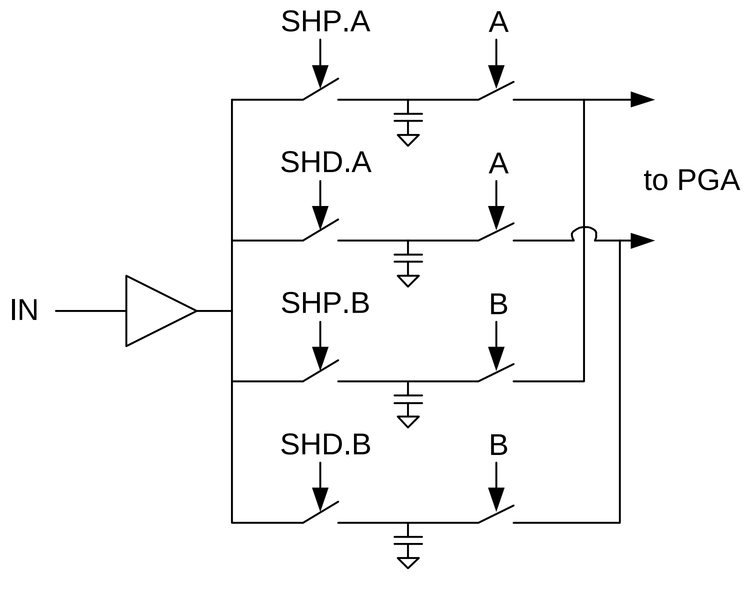


Figure 3. CDS block diagram

1.3.2 Programmable Gain Amplifier

The active video level varies according to the illumination of the scene observed.
In order to ensure that the maximum of the useful dynamic range of the ADC is used even under low light conditions, the video signal is amplified, using this programmable gain amplifier loop (PGA). The gain range is 0dB—36dB.

The amount of gain is adjusted by settings resulting of computation in the DSP and transmitted back to the TDA8787A amplifier by the 3 wires serial interface.

1.3.3 Input DC restoration or Input Bias Level Clamping

The Figure 3 shows the input stage in a common application. The buffered video signal passes through the external coupling capacitor Cin. To restore the DC level to the desired baseline, a clamping circuit is used during the “dummy clamp” period (CLPDM = Low). In all applications, we advice to enable this loop all the time.

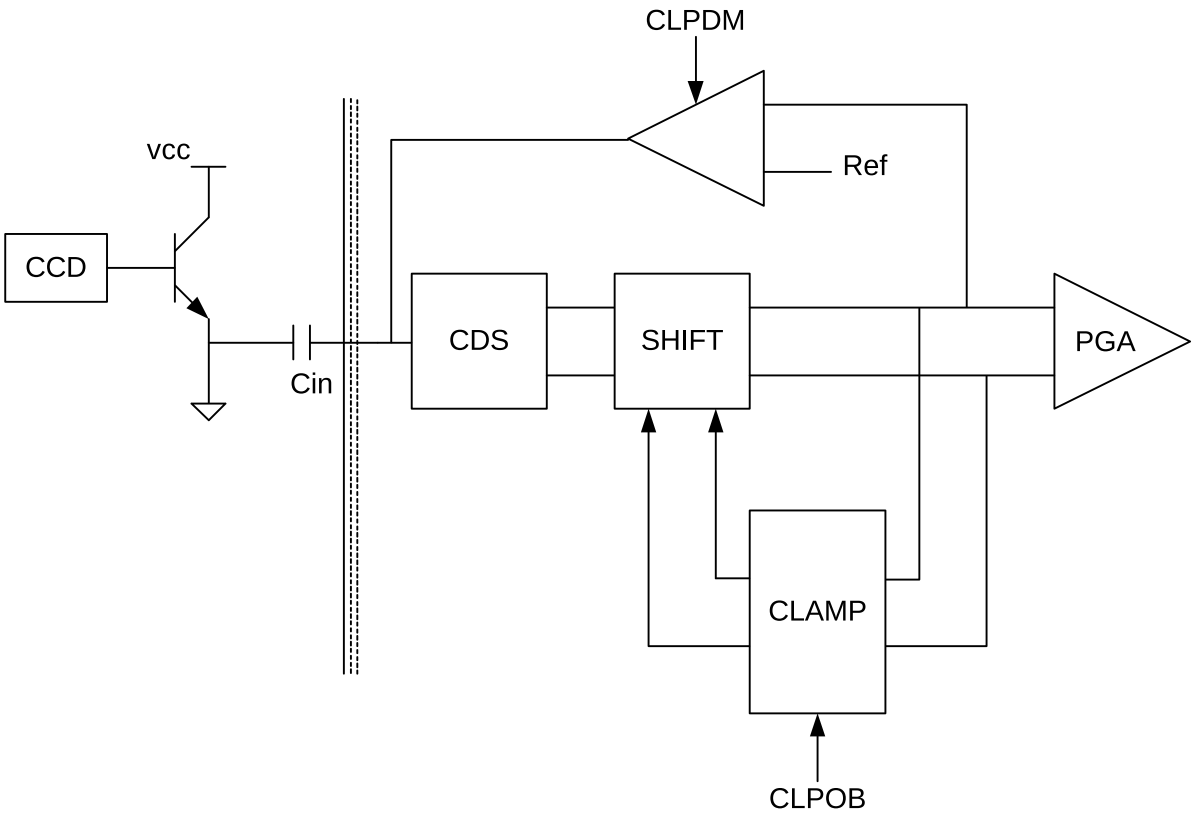


Figure 4. Input Clamp - DC Restoration

1.3.4 Black Level Clamping.

For a good signal processing, the video signal must be referenced to a well established "floating gate level" or "black level". For this operation, the common way is to used the CCD's optical black (OB) pixels, usually at the beginning of the CCD lines, as a calibration level. It is strongly recommended to reserve at least 12 black pixels. During this period, CLPOB active, the black level clamping measures the difference between the input level and the desired reference level. This reference level is programmed by the Serial Interface to set the desired "black color". Of course, this black level offset is applied to both ways of the "ping pong" CDS.
This reference level is hold in the capacitors CPCDS1&2. The calculation of these capacitors is fully dependent of the maximum ripple voltage acceptable and the pixel frequency. The next formula can be used to calculate them:

$CPCDS_{\min} = \frac{I_{Max\_load} * t_{load}}{V_{ripple}}$ with $I_{Max\_load} = 350mA$ at PGA code = 0 and $I_{Max\_load} = 10mA$ at PGA code = 383;

1.3.5 Input Blanking.

In many applications, the IFE is exposed to large input signals, mainly during the "blanking period" and in " CCD shutter high speed" mode. To avoid problems with data processing, the TDA8787A includes a blanking function.
When PBK is active, the digital outputs go to the desired clamp reference level.

1.3.6 OFDOUT function.

To control the substrate bias level of some CCD's, in order to cancelled the smear effect, the TDA8787A provides a voltage control output. This analog output is controlled via the Serial Interface by a 8-bit Digital-to-Analog Converter. The desired value is usually set during the calibration of the camera.

1.4 Serial interface

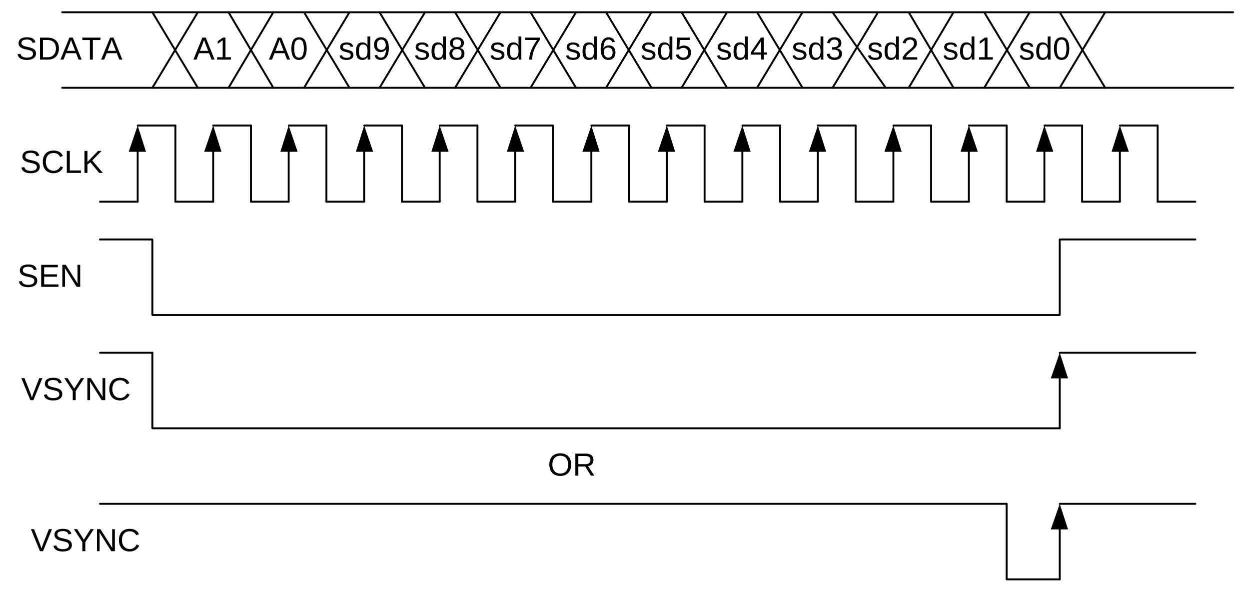
Communication with the configuration register is done through a Serial Interface (SRI).
Just after the "power on" action, a message must be transmitted via the serial interface to the TDA8787A internal registers to set a correct working configuration.
Maximum frequency: 5MHz.

A writing sequence of a serial message is made of 10 data bit + 2 address bit.
A1,A0, SD9,SD8,…,SD2,SD1; with A1 bit first sent.

VSYNC signal can be used to synchronize the registers writing with the Vertical Drive (VD) signal in order to set all the parameters only after a complete image has been displayed. The polarity settings are excluded from the VSYNC latch.
In some applications, this signal can be linked to SEN signal when the firmware takes account of VD.

The setup and hold times, are described in the TDA8787A Data Sheet.

Example:



1.5 Internal registers

The configuration register is programmed to set the requested conditions :

- PGA gain control;
- OFD output control;
- ADC clamp reference control (be careful SD7, SD8 and SD9 must be set to 0;
- Controls pulse polarity settings for SHP, SHD ,CLAMP's, PBK and CLK.

Timing and polarity settings of all these signals, (active edge or level) are given in details in TDA8787A specification and can be summarized in the following tables.

1.5.1 OFD function

Serial address A1A0= 01

Dec	hex	Typical Value of OFD out
0	00	0.0V
255	ff	1.0 V

1.5.2 PGA gain control

Serial address A1A0 = 00. SD9 = 0

Hex	4.5dB +Gain	Bit 8 SD8	Bit 7 SD7	Bit 6 SD6	Bit 5 SD5	Bit 4 SD4	Bit 3 SD3	Bit 2 SD2	Bit 1 SD1	Bit 0 SD0	dec
000	0 dB	0	0	0	0	0	0	0	0	0	0
040	6 dB	0	0	1	0	0	0	0	0	0	64
080	12 dB	0	1	0	0	0	0	0	0	0	128
0C0	18 dB	0	1	1	0	0	0	0	0	0	192
100	24 dB	1	0	0	0	0	0	0	0	0	256
13F	30 dB	1	0	0	1	1	1	1	1	1	319
180	36 dB	1	1	0	0	0	0	0	0	0	383

1.5.3 Control pulses polarity settings

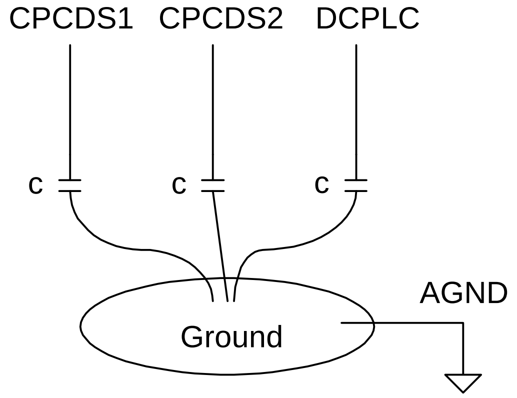
Serial address A1A0 = 11

SD0 =1	SHP, SHD active level HIGH
SD1=1	CLK active edge RISING
SD2=0	CLPDM always active level LOW
SD3=1	CLPOB active level HIGH
SD4 not used	
SD5=1	PBK active level HIGH
SD6=0	VSYNC active edge RISING

2 POWER AND GROUNDING RECOMMENDATIONS

When designing a printed circuit board for application such as PC camera, surveillance cameras, camcorders and digital still cameras, care should be taken to minimize the noise.
For the front end integrated circuit, the basic rules of printed circuit board design and implementation of analog components (such as classical operational amplifiers) must be respected, particularly for power and ground connections.

Firstly, in all cases, we recommend to link the following pins on the same good ground:



The following additional recommendation is given for the CDS input pins which are internally connected to the programmable gain amplifier.

Secondly, the connections between the CCD, the CCD transistor interface and the CDS input should be as short as possible and a ground ring protection around these connections can be beneficial for noise performances.
To separate analog and digital supplies provides the best solution. If it is not possible to do this on the board, then the analog supply pins must be de-coupled effectively from the digital supply pins.

If the same power supply and ground are used for all pins the de-coupling capacitors must be placed as close as possible to the IC package.

In a two-ground system, in order to minimize the noise through package and die parasitic, the following recommendations must be implemented:
All the analog and digital supply pins must be well de-coupled to the analog ground plane.
Only the ground pins associated to the digital outputs must be de-coupled to the digital ground plane. The analog and digital ground planes must be connected together at one point close to the ground pin associated with the digital outputs.
The digital output pins and their associated lines should be shield by the digital ground plane which can be used then as return path for digital signal.

Never use a digital ground plane under analog wires and analog ground plane under digital connections.

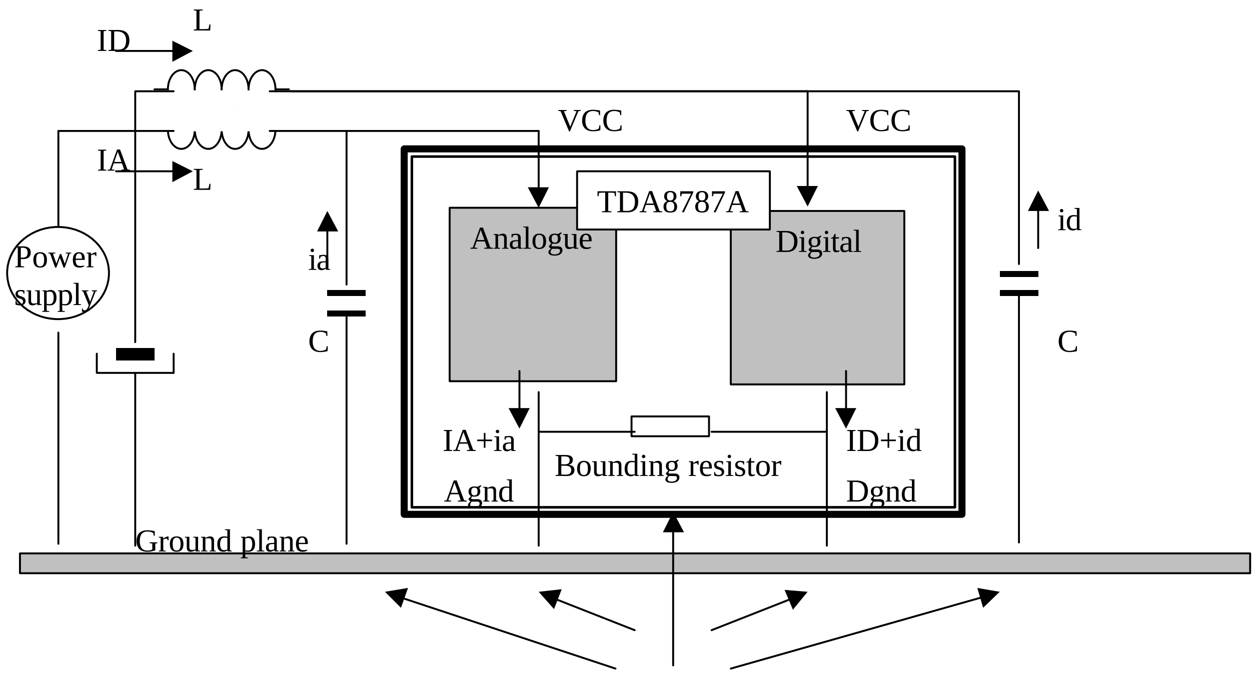


Figure 5. Grounding connections

On the printed board area loop of supply current and impedance of different ground connections must be minimized, the de-coupling capacitors C (ceramic capacitor) must be placed as close as possible to the VCCA and VCCD pins.

Series inductors in power supply lines may be used to improve de-coupling
(E.g. 1…5 µh or BLM components).

Using above de-coupling scheme, both analog and digital supplies can be connected together to a single stable 5 volt supply.

3 FRONT END TYPICAL APPLICATION

The front end IC TDA8787A, used with one SAA 81XX of DSP Philips IC's family, is the core of a high quality video application.
Image sensor, vertical driver, timing generator, micro controller, memories, and DC-DC converter, are the others functions to build a modern CCD video camera

A camdemo is made of two different boards:

- An interface front end also called IFE board.
- A digital processing board.

The whole camera is then made up with the following integrated circuits:

- CCD sensor LZ 2413 for standard NTSC LZ2423 for PAL standard
- Vertical Driver (VD) LR36683
- Pulse Pattern Generator (PPG) LZ95G55
- Front End for analog processing and digitalization TDA8787A (FE)
- Digital Signal Processing and formatting (DSP) SAA8112
- Video encoder SAA7102
- Memory EEPROM PCD8594

In addition on the IFE schematic, we find:

- 2 simple small SMPS stages to transform the 5 volts power battery voltage into +15Volts and -8Volts needed to bias the CCD and Vertical Driver devices.
- One transistor buffer stage to interface the CCD with the FE;
- One non inverting amplifier stage to translate the OFDOUT signal of the FE to the FD input of the CCD;
- One push pull stage to transform the OFDX signal of the PPG into a high voltage pulse command added to the OFD on the FD CCD input (shutter function).

These boards are connected together by a connector in order to be able to mix different configurations of our circuits (TDA8784+SAA8112 or TDA8787A+SAA8112 …).

In a previous application note, AN97037, evaluation board for camera more details can be found about the description of this concept.

This present application has been modified in the front-end part only to become compatible with the TDA8787A circuit.

For people non-familiar with the DSP SAA81xx IC's family, it is recommended to read this previous document to get better understanding of the DSP SAA8112 performance.

If there is no basic change for the system point of view due to the substitution of the TDA8784 by TDA8787A, the use of new TDA 8787A circuit improves the global performance of the basic application: more simple connection with the PPG, lower noise, possible choice of the pulse polarity by software, lower power consumption and less external components.

3.1 Interface connector pinning

In the description list below and in the IFE diagram:

- DS = DSP SAA8112
- UC = micro-controller implemented in the SAA8112
- EE = Eeprom
- JB = I2C / UART connector
- JD = digital output connector

Names on connector

1	+5 V	2	+5 V
3	GND	4	GND
5	UC5 P1-3	6	UC4 P1-2
7	UC2 P1 –0	8	CLK1
9	CLK2	10	VD UC14 P3-2
11	UC7 P1-5 PAL/NTSC	12	HD UC16 P3-4
13	UC29 P2-5	14	FI UC18 P3-6
15	UC28 P2-4	16	GND
17	UC27 P2-3	18	+5 V n.u.
19	UC26 P2-2	20	UC25 P2-1
21	P1 INPUT	22	SMPS
23	P0 INPUT	24	DATA 9
25	DATA 8	26	DATA 7
27	DATA 6	28	+5V n.u.
29	DATA 5	30	GND
31	DATA 3	32	DATA 4
33	DATA 1	34	DATA 2
35	SCLK INPUT	36	DATA 0
37	SDATA INPUT	38	SEN
39	STAND BY TDA	40	DACOUT
41	GND	42	GND
43	+5V	44	5 +V

Names on micro-controller

BIT	NAME	DESCRIPTION
P0.0	SCLE	I2C bus clock for EEPROM
P0.1	SDAE	I2C bus data for EEPROM
P1.3	PPR_OEN	TDA8787A Output Enable Not
*P1.5	TVMD	PPG mode select
P1.6	SCLM	I2C bus clock for MMI
P1.7	SDAM	I2C bus data for MMI
P2.0	PP_STDBY	TDA8787A standby pin
P2.1	ACLXP	PPG internal reset (all clear)
P2.2	EEUD	PPG Electric Exposure 2
P2.3	EENR	PPG Electric Exposure 3
P2.4	SMD1	PPG Shutter control 1
P2.6	POR	POR for DSP
P3.0	SNDA	SNERT bus data for DSP
P3.1	SNCL	SNERT bus clock for DSP
P3.2	VD	VD interrupt input
*P3.6	FI	PPG Field Index
P3.7	SNRST	SNERT bus reset for DSP

3.2 Electrical diagrams

Reported in enclosures.

3.3 Optical-mechanical block

In the front of the TDA8787A there is a CCD sharp LZ2413 which is a ¼ type solid state image sensor having 542*498 pixels. This CCD is compatible with the NTSC standard. For a PAL application this CCD can be changed and directly replaced by the LZ2423 CCD type but in this case the quartz oscillator must be also changed:

- 19.06993 MHz is used for NTSC standard;
- 19.3125 MHz is used for PAL standard;

In the same time, the declaration of NTSC or PAL standards must be swapped in the setting of the DSP program and all parameters concerning the active and black windows pixels must be updated. It can be done with the Graphic User Interface (GUI) developed in our US laboratory, to demonstrated the SAA8112 possibilities (Reference N°2).

In the front of the CCD, there is a optical low pass filter from American KSS, Inc.
This particular filter is currently being produced by this manufacturer under the reference OG-BF389 (3122 168 7514.0), the size of this infrared filter is 7.75*7.25*3.27 mm and must be introduced in the optical block as shown below.

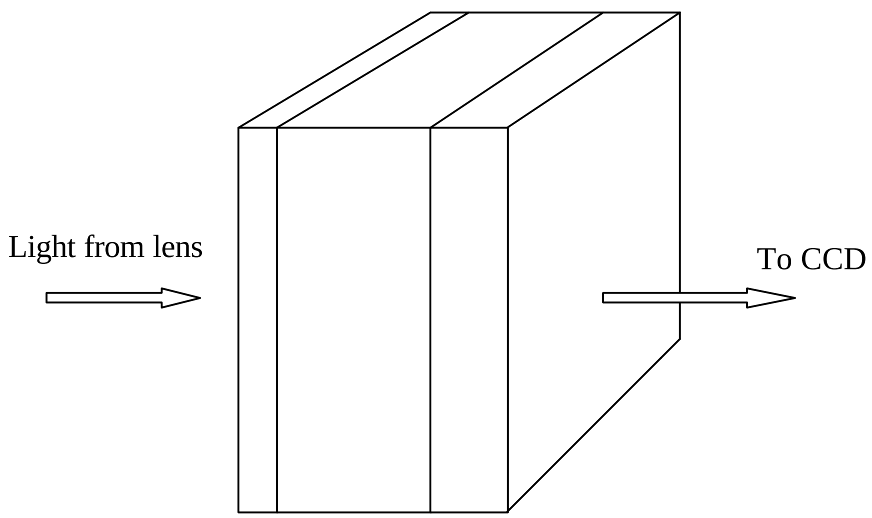


Figure 6. Optical filter

In addition each kit is containing the following elements:

- 1 piece CS mount interface
- 1 piece under-plate
- 1 piece CS mount ring
- 1 piece retaining ring
- 1 piece filter foan
- 2 screws M2.5.

The IFE kit can be delivered with CS CCTV lens coming from different suppliers.

Lens which generally are 4mm F 1.2 or 8 mm F1.2 depending available material in stock.

Documentation on these elements are available on request.

4 ENCLOSURES

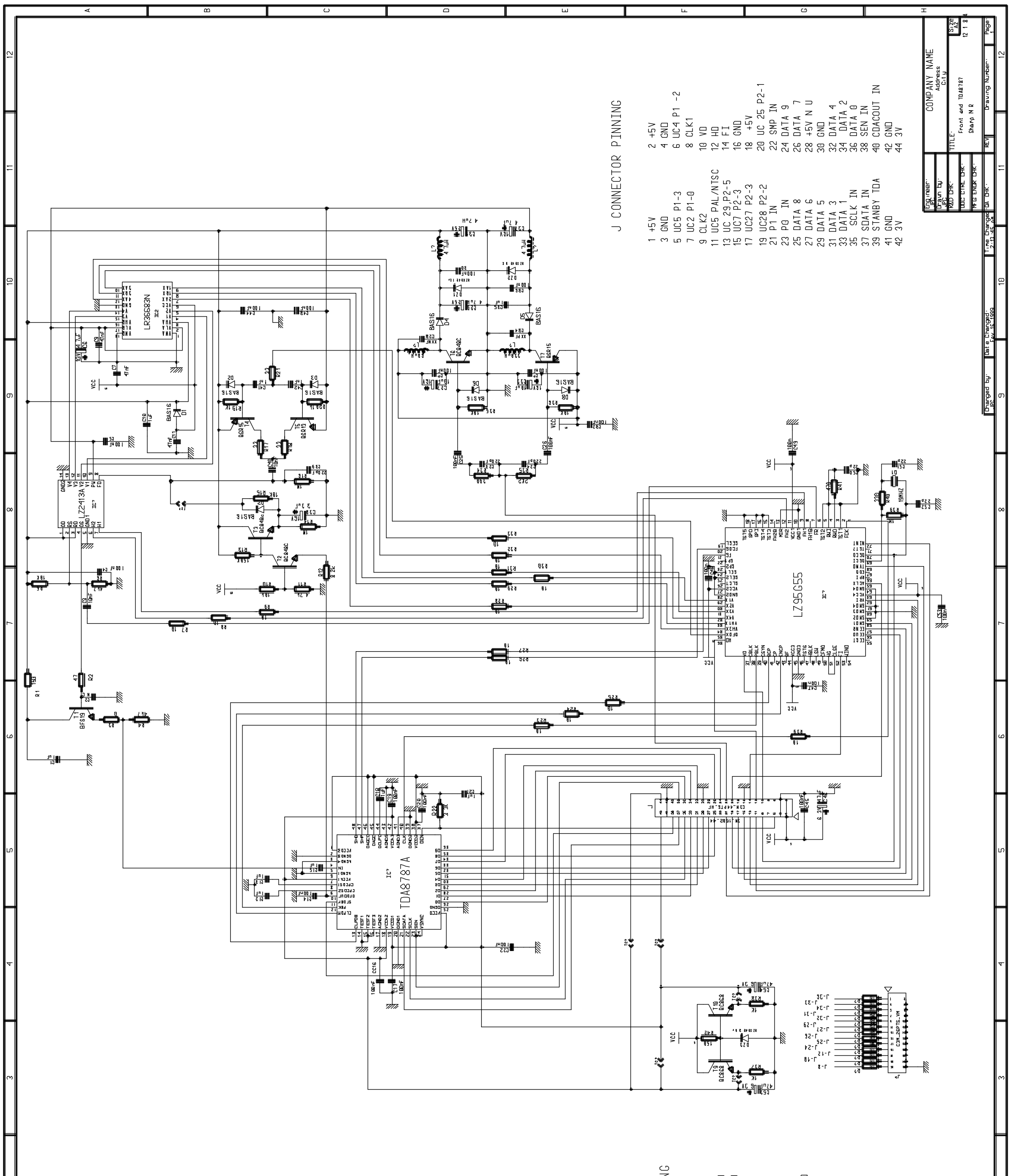

J CONNECTOR PINNING
1 +5V
2 +5V
3 GND
4 GND
5 UC5 P1-3
6 UC4 P1 -2
7 UC2 P1-0
8 CLK1
9 CLK2
10 VD
11 UC5 PAL/NTSC
12 HD
13 UC 29 P2-5
14 FI
15 UC7 P2-3
16 GND
17 UC27 P2-3
18 +5V
19 UC28 P2-2
20 UC 25 P2-1
21 P1 IN
22 SMP IN
23 P0 IN
24 DATA 9
25 DATA 8
26 DATA 7
27 DATA 6
28 +5V N U
29 DATA 5
30 GND
31 DATA 3
32 DATA 4
33 DATA 1
34 DATA 2
35 SCLK IN
36 DATA 0
37 SDATA IN
38 SEN IN
39 STANBY TDA
40 CDACOUT IN
41 GND
42 GND
42 3V
44 3V
J2 CONNECTOR PINNING
1 DATA 0
2 GND
3 DATA 1
4 GND
5 DATA 2
6 GND
7 DATA 3
8 GND
9 DATA 4
10 GND
11 DATA 5
12 GND
13 DATA 6
14 GND
15 DATA 7
16 GND
17 DATA 8
18 GND
19 DATA 9
20 GND
21 HD
22 GND
23 VD
24 GND
25 CLOCK1
26 GND
TDA8787A
LZ95G55

Figure 7. Electrical schematic

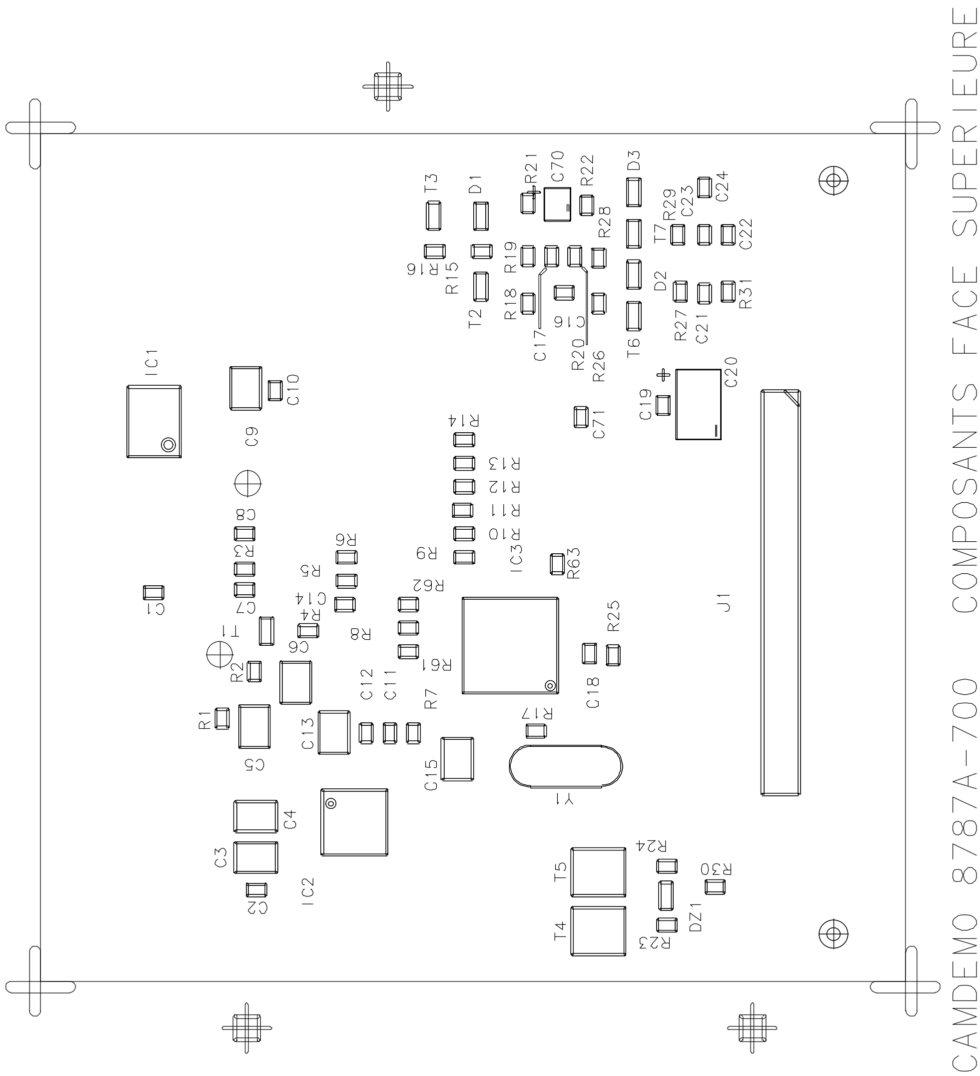


Figure 8. Components implementation upper side

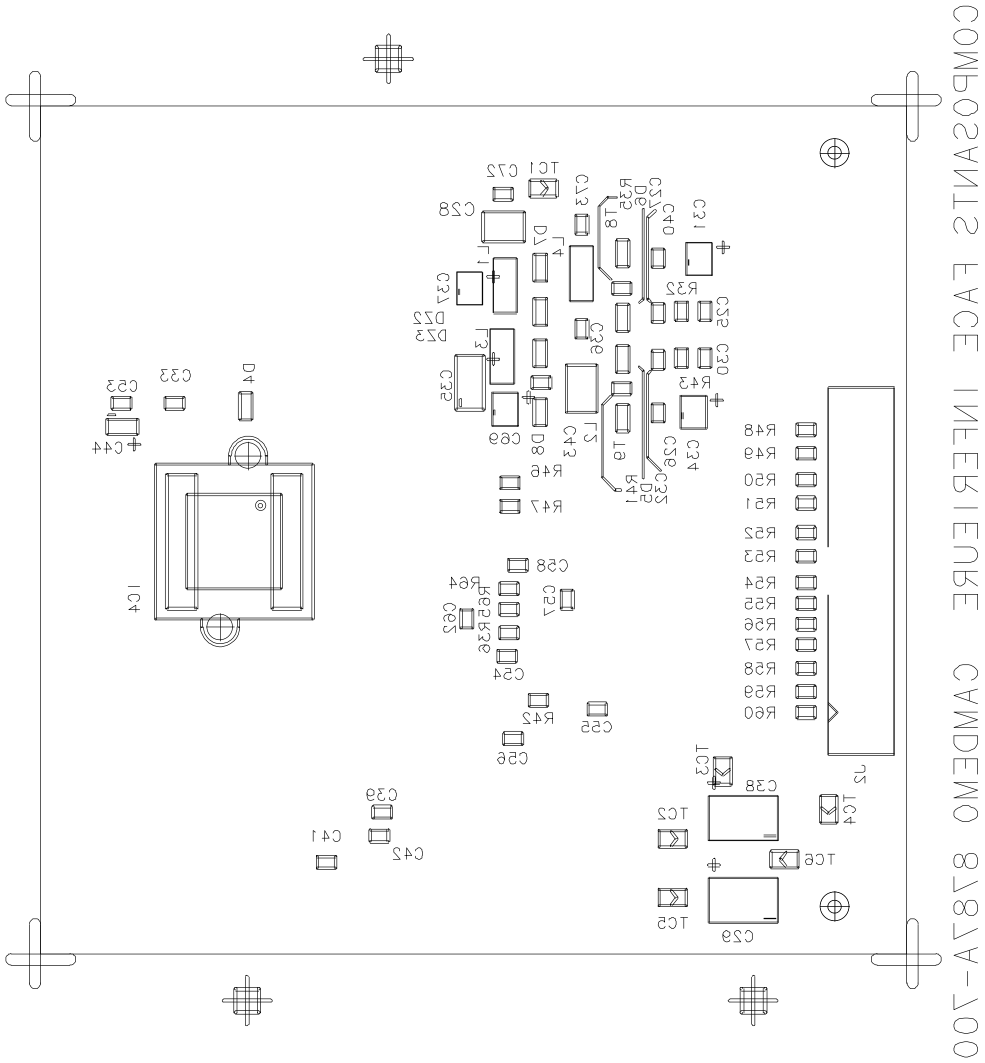


Figure 9. components implementation lower side

5 REFERENCES

1) Application Note AN97037 – May 1992
Camera evaluation board documentation SDA8112-TDA8786
Author: Stephane Desproges

2) Addendum to AN97037 – June 1997
Camera I’C controller software documentation and user manual
Author: Jürgen Krehnke

3) Caen Team Design – Internal Note
Authors: S. Jacquet, R. Morisson

4) Software for TDA8787A, version V3.12
(Modification of V3.11 for TDA8786 by C. Kohler and H. Jacquemin) .

6 LIST OF FIGURES

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